Amendments to the Claims:

Rewrite the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. – 11 (canceled)

12. (currently amended) A memory architecture comprising:

a plurality of level one ~~cache~~ caches each comprising texel information and each associated with a corresponding graphics pipeline;

~~a~~ a common level two cache, operatively coupled to each of the plurality of level one ~~cache~~caches, that comprises overlapping fetched texel information resulting from execution of previous memory fetch instructions, wherein the previous memory fetch instructions resulted in storage of requested texel information in at least one corresponding level one cache of the plurality of level one caches;

wherein when a particular level one cache of the plurality of ~~the~~ level one ~~cache~~ caches does not comprise overlapping fetched texel information requested by a subsequent memory fetch instruction, the level two cache is operative to transmit the overlapping fetched texel information requested by the subsequent memory fetch instruction to the particular level one cache of the plurality of level one ~~cache~~caches; and

wherein ~~each of the previous memory fetch instructions and~~ the subsequent memory fetch instruction ~~result~~ results in storage of requested texel information at least in the particular level one cache of the plurality of level one caches.

13. (currently amended) The memory architecture of claim 12, wherein:

each level one cache of the plurality of level one ~~cache~~ caches comprises a plurality of texture cache blocks; and

wherein one of the plurality of texture cache blocks is operative to receive the subsequent texel fetch instruction.

14. (currently amended) The memory architecture of claim 12, further comprising:

a main memory operatively coupled to the level two cache; and

wherein when the particular level one cache of the plurality of level one caches and the level two cache do not comprise texel information requested by a second subsequent memory fetch instruction, the main memory is operative to transmit the texel information requested by the second subsequent memory fetch instruction to the level two cache for storage.

15. (currently amended) The memory architecture of claim 14, wherein the level two cache transmits the texel information requested by the second subsequent texel fetch instruction to the particular level one cache of the plurality of level one caches for storage.

16. (currently amended) A graphics processing device, comprising:

a graphics controller operative to execute memory fetch instructions;

a main memory;

a plurality of level one ~~cache~~ caches each coupled to the graphics controller, each ~~the level one cache~~ comprising texel information, and each associated with a corresponding graphics pipeline; and

a level two cache coupled between the main memory and the plurality of level one ~~cache~~caches, the level two cache comprising overlapping fetched texel information resulting from execution of previous memory fetch instructions, wherein the previous memory fetch

instructions resulted in storage of requested texel information in at least one corresponding level one cache of the plurality of level one caches;

wherein when a particular level one cache of the plurality of level one ~~cache~~ caches does not comprise overlapping fetched texel information requested by a subsequent memory fetch instruction, the level two cache transmits the overlapping fetched texel information requested by the subsequent memory fetch instruction to the particular level one cache of the plurality of level one caches; and

wherein ~~each of the previous memory fetch instructions and~~ the subsequent memory fetch instruction ~~result~~ results in storage of requested texel information at least in the particular level one cache of the plurality of level one caches.

17. (previously presented) The graphics processing device of claim 16, wherein the graphics controller is operative to request the subsequent memory fetch instruction.

18. (previously presented) The graphics processing device of claim 17, wherein the graphics controller comprises a plurality of fetch blocks, wherein one of the plurality of fetch blocks is operative to request the subsequent memory fetch instruction.

19. (currently amended) The graphics processing device of claim 17, wherein the particular level one cache of the plurality of level one caches transmits the overlapping fetched texel information requested by the subsequent memory fetch instruction to the graphics controller.

20. (currently amended) The graphics processing device of claim 16, wherein

each of the plurality of level one ~~cache~~ caches comprises a plurality of texture cache blocks; and

wherein one of the plurality of texture cache blocks is operative to receive the subsequent texel fetch instruction.

21. (currently amended) The graphics processing device of claim 16, wherein when the particular level one cache of the plurality of level one caches and the level two cache do not comprise texel information requested by a second subsequent memory fetch instruction, the main memory is operative to transmit the texel information requested by the second subsequent memory fetch instruction to the level two cache for storage.

22. (currently amended) The graphics processing device of claim 21, wherein the level two cache transmits the texel information requested by the second subsequent texel fetch instruction to the particular level one cache of the plurality of level one caches for storage.